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Fabrication and characterization of Au/SBT/LZO/Si MFIS structure

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Abstract Ferroelectric $SrBi_2Ta_2O_9$ (SBT) films on a p-type Si (100) wafer with a $LaZrO_x$ (LZO) buffer layer have been fabricated to form a metal-ferroelectric-insulator–semiconductor (MFIS) structure. The LZO thin film and SBT films were deposited by using a sol–gel method. The equivalent oxide thickness (EOT) value of the LZO thin film was about 8.83 nm. Also, the leakage current density of the LZO thin film is about 3.3×10^{-5} A/cm^2 at bias sweeping voltage of ±5 V. SBT films were crystallized in polycrystalline phase with highly preferred (115) orientation. Also, the intensity of each pick slightly increased as thickness of SBT films increased. The *C*–*V* characteristics of Au/SBT/LZO/Si structure showed clockwise hysteresis loop. The memory window width increased as the thickness of SBT films increased. The leakage current density of Au/SBT/LZO/Si structure decreased as thickness of SBT films increased.

Keywords $SrBi_2Ta_2O_9$ · $LaZrO_x$ · MFIS · Sol–gel

1 Introduction

One-transistor (1-T) ferroelectric random access memory (FRAM) has widely investigated as one of the next generation non-volatile memories since it has superior advantages such as high-density integration and non-destructive read-out operation as well as low power-consumption and high-speed operation [1, 2]. However, when the ferroelectric thin film is directly deposited on a silicon substrate, severe interfacial problems, such as interdiffusion, low-k oxide layer formation or crystalline quality degradation arise [3]. The metal-ferroelectric-insulator–semiconductor (MFIS) structure where the buffer insulator is inserted at the interface between the ferroelectric layer and Si substrate, has been proposed as a solution for interfacial problems [4].

Most insulators investigated as a buffer layer in an MFIS structure are high-k dielectric materials such as Ta_2O_5, ZrO_2, HfO_2, $HfAlO_x$ or Y_2O_3 [5–9]. The $LaZrO_x$ (LZO) thin film has been recently reported to have a high dielectric constant of ≈20 and be chemically stable in contact with Si [10]. Further, it has been reported that the LZO has a cubic pyroclore structure with a lattice parameter, which leads to a mismatch of 0.68% with Si ($2a_{Si}$=10.86 Å) [11]. In particular, both lanthanum and zirconium atoms, the constituents of the $LaZrO_x$ thin film, have been considered to be thermally stable in contact with Si [10]. Thus, we can expect that the LZO thin film act as a good buffer insulator in an MFIS structure.

As a ferroelectric layer for an MFIS structure, we chose the $SrBi_2Ta_2O_9$ (SBT) film among several ferroelectric materials such as $Pb(Zr,Ti)O_3$, $Bi_4Ti_3O_{12}$, $(Bi,La)_4Ti_3O_{12}$ or $Pb_5Ge_3O_{11}$ [12–15]. The SBT film is one of the most promising candidates for 1-T type FRAM because of its high fatigue endurance, good retention and low leakage current [16].

In this study, we fabricated the LZO/Si and the SBT/LZO/Si structures using a sol–gel method, and then characterized the physical and electrical properties of each structure. From these measurements, we evaluated the SBT/LZO/Si structure for FRAM.

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2 Experiments

To fabricate the SBT/LZO/Si structure, we deposited the LZO thin film and the SBT film on the Si substrate using a sol–gel method. The LZO (i.e., molar ratio of La/Zr=1) solution of 0.1 M concentration and the $Sr_{0.9}Bi_{2.1}Ta_2O_9$ solution of 0.3 M concentration were prepared, respectively.

After removing the native oxide layer from the surface of Si by soaking into a buffered oxide etchant (BOE), we spin-coated the LZO solution on a p-type Si(100) wafer at 4000 rpm for 25 s. The coated LZO thin film was annealed at 750°C for 30 min in O_2 atmosphere by rapid thermal annealing (RTA).

The SBT film was deposited on the LZO/Si structure to form a SBT/LZO/Si structure. The SBT solution was also spin-coated at 3000 rpm for 20 s and dried at 250°C for 10 min on a hot-plate. After several repetitions of these coating and drying procedures to obtain the desired thickness, the films were finally crystallized at 800°C for 30 min in O_2 atmosphere by RTA. For electrical measurements, Au electrodes were fabricated onto the samples using shadow mask by a thermal evaporation.

The surface morphology and crystallization quality of the LZO thin film and the SBT film were observed by atomic force microscopy (AFM) and X-ray diffraction (XRD) measurement, respectively. The capacitance–voltage (*C*–*V*) and leakage current density–voltage (*J*–*V*) characteristics of Au/SBT/LZO/Si structure were measured using HP 4280A capacitance-meter and HP 4155C precision semiconductor parameter analyzer, respectively.

3 Results and discussion

Figure 1 shows the surface morphological image of the LZO thin film measured by AFM. The measured area was 500×500 nm^2. The average and root-mean-squared (RMS) surface roughness of LZO film were about 0.284 nm and 0.359 nm, respectively. The surface roughness of a buffer layer is very important because the surface structure of a buffer insulator affects the electrical properties of the MFIS

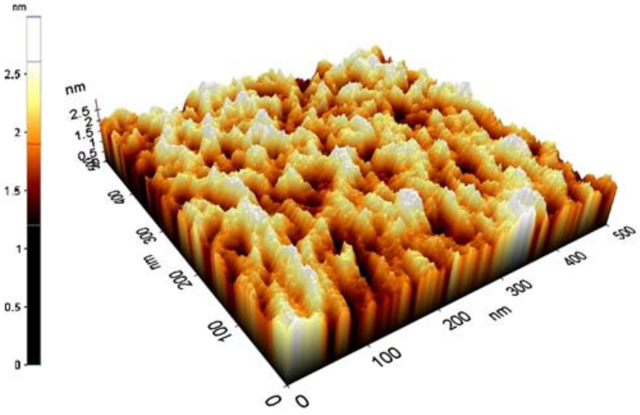

Fig. 1 Surface morphological image of the LZO film annealed at 750°C

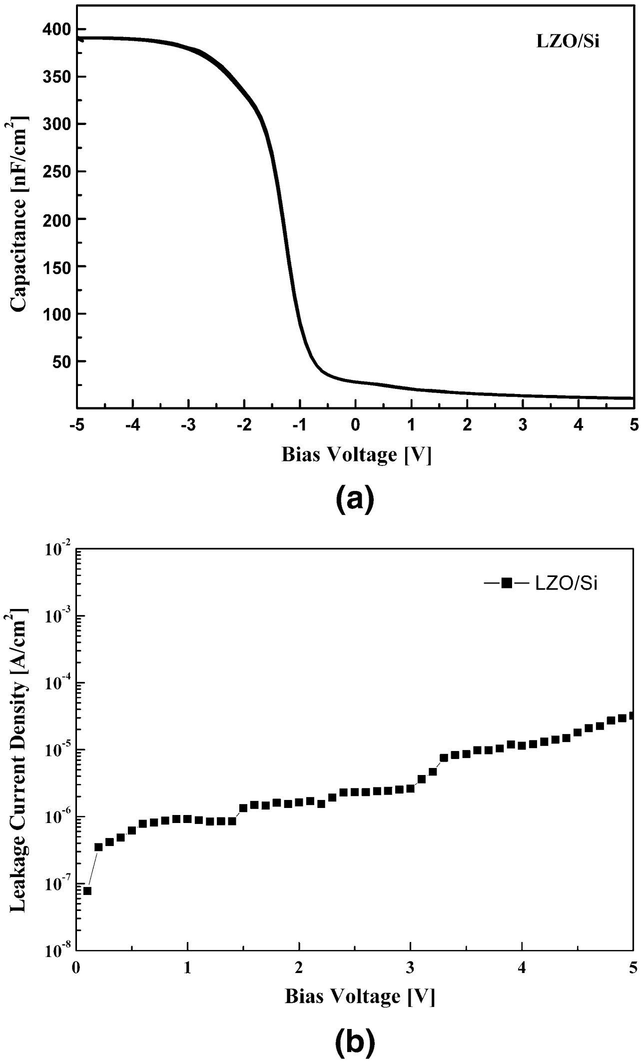

Fig. 2 (**a**) *C*–*V* and (**b**) *J*–*V* characteristics of the 750°C-annealed LZO/Si structure

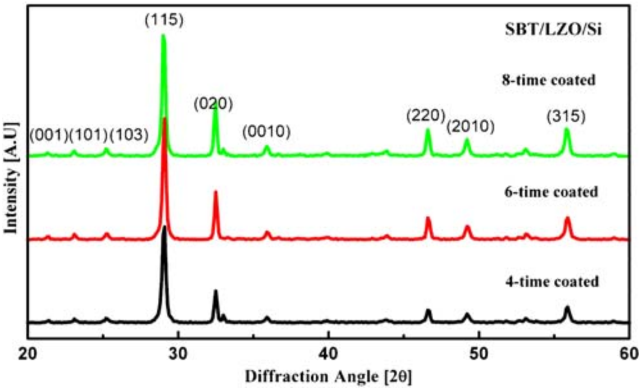

Fig. 3 Typical X-ray diffraction patterns of SBT films with different thickness

structure. The deposited LZO film had very flat and smooth surface morphologies.

Figure 2 shows *C–V* and *J–V* characteristics of the LZO thin film annealed at 750°C. The equivalent oxide thickness

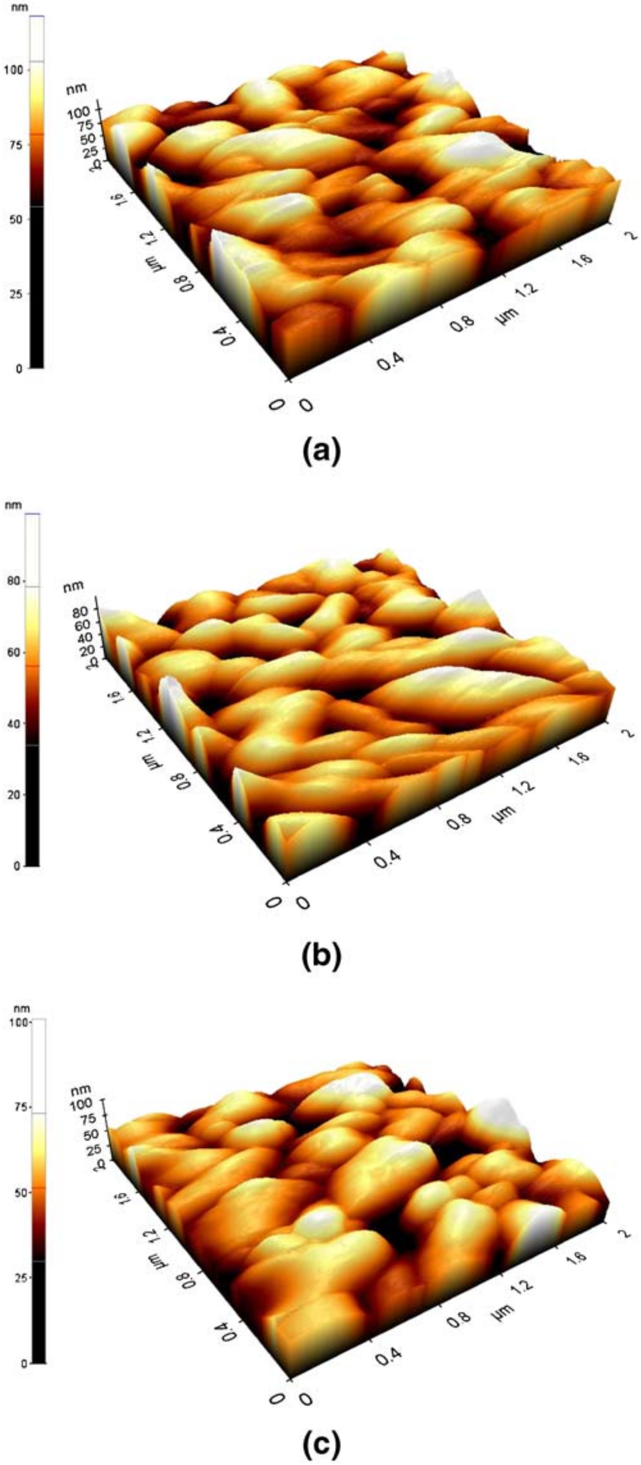

Fig. 4 Surface morphological images of SBT films with different thickness: (**a**) four-time coated film (**b**) six-time coated film (**c**) six-time coated film

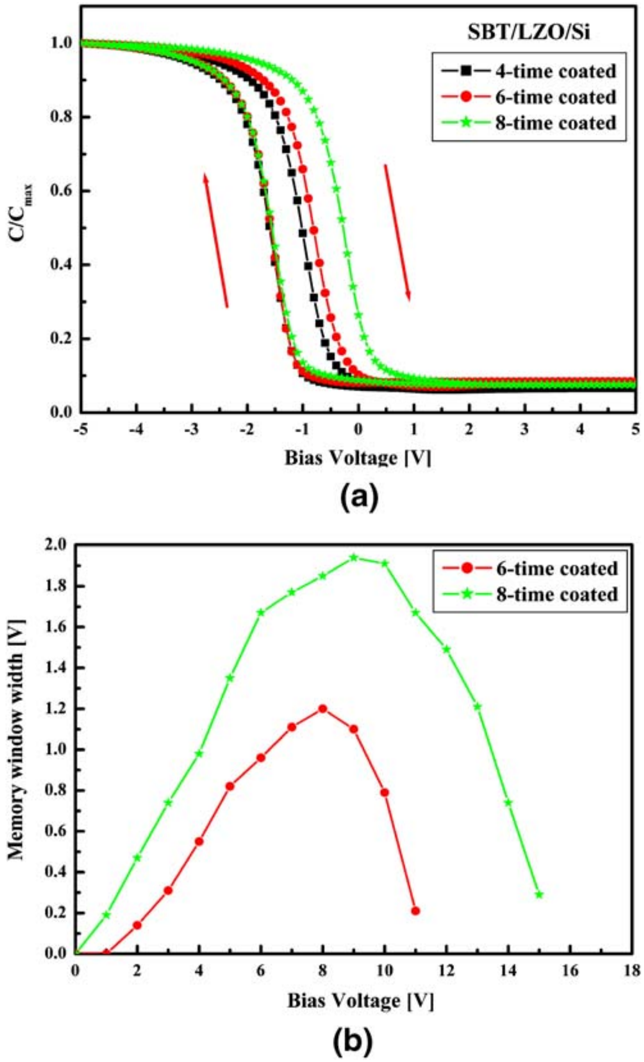

Fig. 5 (**a**) *C–V* characteristics and (**b**) memory window width variations of SBT/LZO/Si structures according to the thickness of SBT films

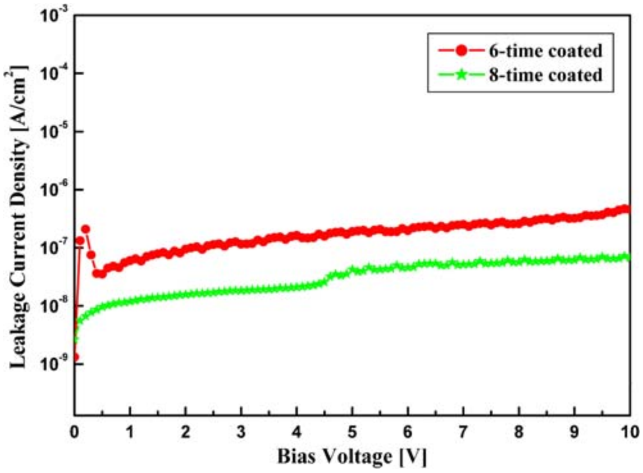

Fig. 6 *J–V* characteristics of the SBT film with different thickness on LZO/Si structure

(EOT) value was about 8.83 nm determined from the accumulation capacitance value. This demonstrates that the LZO film has the appropriate accumulation capacitance and small EOT value. The leakage current density was about 3.3×10^{-5} A/cm^2 at 5 V. No hysteresis was observed in the *C–V* curve, which demonstrated that there is little chance for a rechargeable oxide trap to exist at the interface between the LZO film and the Si substrate.

Figure 3 shows the XRD patterns of SBT films with different thickness. All samples were deposited on LZO/Si structures and annealed at 800°C. Thickness was controlled by coating times, i.e. four-time, six-time and eight-time coating, and then measured respectively. It was revealed from the figure that all SBT film were crystallized in a polycrystalline phase with a highly preferred (115) orientation. The intensity of each pick slightly increased as thickness of SBT films increased. In general, film orientation is one of the important factors for ferroelectric properties, such as polarization, because it is related to direction of dipoles [17]. The magnitude of remanent polarization depends on the orientation of ferroelectric film and then affects the characteristic of it.

The surface morphology of the SBT films with different thickness is illustrated in Fig. 4. The measured area was 2×2 μm^2. The RMS surface roughness values of SBT films on LZO/Si structure were about 12.471 nm, 11.373 nm and 11.097 nm for four-time, six-time and eight-time coated films, respectively. The roughness slightly decreased as SBT films increased but the variation of the roughness was negligible.

Figure 5 (a) shows high-frequency (1 MHz) *C–V* characteristics of Au/SBT/LZO/Si structures according to the thickness of SBT films. For comparison, capacitance values were normalized. As shown in the figure, hysteresis loops with a clockwise trace as indicated by arrows were observed, which related with the ferroelectric behavior of the SBT film. In Fig. 5 (b), the memory window width increased as the bias voltage increased and the thickness of SBT films increased. The maximum value of memory window width was about 1.2 V at bias sweep voltage ±8 V for the six-time coated SBT film, whereas, 1.94 V at bias sweep voltage ±9 V for the eight-time coated one. These results demonstrate that the bias voltage was sufficiently distributed to the SBT film deposited on LZO/Si structure. In general, insulators as a buffer layer have to take enough large accumulation capacitance and small EOT in order to appropriately distribute bias voltage to the ferroelectric layer in an MFIS structure. Therefore, we assured that the LZO film was applicable as a buffer layer between the SBT film and the Si substrate.

Figure 6 shows *J–V* characteristics of the SBT film with different thickness on the LZO/Si structure with a sweep rate 0.1 V/s. The leakage current density was lower than 1×10^{-6} A/cm^2 and 1×10^{-7} A/cm^2 at 10 V for each samples. The measured values of leakage current density, as one of the most important properties for an MFIS structure, show relatively the good characteristic. From this fact we deduce that interfacial properties of an MFS structure were improved by using LZO buffer layer.

4 Conclusions

We fabricated an MFIS structure of Au/SBT/LZO/Si using the SBT film as a ferroelectric layer and the LZO film as an insulating buffer layer. *C–V* and *J–V* characteristics of the LZO film revealed that the sol–gel deposited LZO thin film annealed at 750°C had good electrical properties. The EOT value of LZO thin film was about 8.83 nm. Also, the leakage current density of LZO thin film was about 3.3×10^{-5} A/cm^2. AFM image of the LZO film showed a very flat and smooth surface. The SBT films on LZO/Si structure were crystallized in polycrystalline phase with highly preferred (115) orientation. The *C–V* characteristics of Au/SBT/LZO/Si structures showed clockwise hysteresis loops. The memory window width increased as the bias voltage and the thickness of SBT films increased. The leakage current densities were lower than 1×10^{-6} A/cm^2 and 1×10^{-7} A/cm^2 at 10 V for the six-time coated and eight-time coated SBT films, respectively.

From these results, we confirmed the LZO thin film in the Au/SBT/LZO/Si structure worked well as the role of a buffer layer. Consequently, the MFIS structure with a LZO buffer layer would be suitable for ferroelectric random access memory application.

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